

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-310509

(43)Date of publication of application : 04.11.1994

(51)Int.Cl.

H01L 21/3205

(21)Application number : 05-095666

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(22)Date of filing : 22.04.1993

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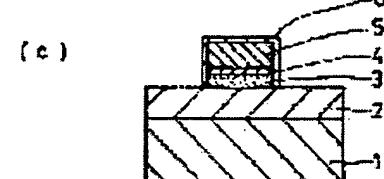
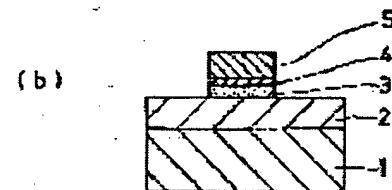
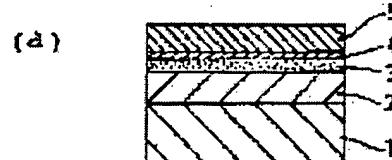
(54) WIRING STRUCTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:

PURPOSE: To completely prevent a diffusion of Cu into surrounding SiO₂ and Si by a method wherein a barrier layer not solidifying Cu in the base or periphery of a Cu wiring is provided and a trap layer completely solidifying Cu in the base or periphery of this barrier layer is provided:

CONSTITUTION: An insulation film 2 is provided on the surface of a Si substrate 1 and a Mn film 3 forming a trap layer grows on the surface as a base of a Cu film.

Further, a W film 4 forming the barrier layer grows and Cu grows on the surface and these are patterned to form a Cu wiring. W is selectively grown by a CVD method only in the periphery of this Cu wiring and the base film to form a W coated film 6. Thus, it is possible to realize a Cu wiring structure of a semiconductor capable of restricting a diffusion of Cu.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than

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[Date of final disposal for application]

[Patent number]

[Date of registration]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the wiring structure of a semiconductor integrated circuit (LSI).

[0002]

[Description of the Prior Art] Now, what is depended on an alloy with aluminum, aluminum and Si, or Cu as a wiring material of a semiconductor integrated circuit is used. In order to use aluminum as a main material in such wiring, allowable-current density is $x(2-3) 105 \text{ A/cm}^2$. It was restricted to below. The reason is because wiring is disconnected by electromigration, when the current exceeding this is passed. In order to pass more current, the alloy which contains 0.1 - 5% of Cu in aluinum as a material of wiring may be used. However, although allowable-current density improves, the specific resistance of wiring increases and the problem of the reliability fall accompanying generation of heat produces it.

[0003] On the other hand, instead of aluminum wiring, using Cu substantially as a high wiring material of electromigration resistance is proposed. However, it compares with aluminum and Cu film is Si or SiO₂. It is easy to be spread in inside, therefore the problem of barring normal operation of a transistor arises. The application as a diffusion prevention layer of Cu using the barrier material of former various kinds has been proposed (JP,63-156341,A, JP,1-202841,A, etc.). However, it is difficult to suppress diffusion of Cu completely with such technology.

[0004]

[Problem(s) to be Solved by the Invention] Therefore, Cu which passed the barrier layer is captured effectively and the wiring structure of capturing Cu diffused slightly is needed. Namely, SiO₂ of the circumference Or development of the wiring structure where diffusion of Cu to the inside of Si can be prevented completely is pressing need.

[0005]

[Means for Solving the Problem] In order that this invention may solve the aforementioned trouble, Cu and the barrier layer not dissolving are prepared in the ground or the circumference of Cu wiring, and Cu wiring structure characterized by preparing Cu and the trap layer which dissolves completely in the ground or the circumference of this barrier layer is proposed.

[0006]

[Function] The barrier layer in contact with Cu needs to excel in the diffusion prevention effect of Cu, and not to raise resistance of Cu. Since Ta, W, or a Ta-W alloy does not dissolve with Cu, it does not raise the specific resistance of Cu to heat treatment, and since the self-diffusion coefficient is small compared with other transition metals, such as Nb, Mo, Cr, and Ti, it is effective as a diffusion prevention material of Cu.

[0007] The trap layer in contact with a barrier layer captures Cu which passed the barrier layer. Since Bi, Ga, Mg, Mn, etc. dissolve completely with Cu, if a trap layer is prepared by these, they will form Cu and the solid solution which passed the barrier layer, and will capture Cu in a trap layer. If the conventional wiring structure of having only a barrier layer with the same thickness as the thickness which doubled

the wiring structure, and a barrier layer and a trap layer of this invention which has a barrier layer and a trap layer compares the amount of Cu(s) diffused around, the diffusion prevention effect excellent in the structure of the former by this invention will be seen.

[0008]

[Example] An example is raised to below and detailed explanation is given to it. Table 1 shows Cu concentration on the front face of Si by SIMS, after carrying out diffusion heat treatment of the cascade screen of Cu/M1/M2 / Si (an M1 = barrier layer, M2 = trap layer) for the purpose of the barrier nature evaluation to Cu of various barrier material. These multilayers make 900Å of barrier layer membranes deposit by RF magnetron sputtering on Si substrate, and carry out 10000Å laminating of the Cu by RF magnetron sputtering further. Heat treatment is a multilayer H2 700 degree-Cx3h was carried out in inside.

[0009] When barrier material is made into a laminated structure with the trap material of Ta, W and Mg, or Mn compared with the case where it considers as Ta or Zr single phase proposed until now, it turns out that Cu concentration existing, the circumference, i.e., Si substrate front face, of a barrier layer, is decreasing. This is considered that Cu element which passed the barrier layer dissolves to Mg or Mn, and the diffusion to Si substrate is suppressed effectively by the latter. Since Ta or W which is a barrier layer did not dissolve with Cu at this time, elevation of sheet resistance of a sample was not observed.

[0010] Drawing 1 shows the cross section of Cu wiring structure by this invention. drawing 1 (a) -- like -- the front face of the Si substrate 1 -- the insulator layer 2 of 5000Å BPSG -- preparing -- the front face -- 200Å of Mn films 3 is grown up by 5Å/s in membrane formation speed by RF magnetron sputtering in Ar atmosphere of total pressure 2mTorr the whole surface on BPSG as a ground of Cu film Furthermore, 400Å of W films 4 is grown up by 10Å/s in membrane formation speed by RF magnetron sputtering in Ar atmosphere of total pressure 2mTorr. 5000Å of Cu(s) is grown up by 60Å/s in membrane formation speed by RF magnetron sputtering in Ar atmosphere of total pressure 2mTorr, like drawing 1 (b), patterning of this is carried out to the front face, and the Cu wiring 5 is formed in it. Still like drawing 1 (c), 400Å W is alternatively grown up only into the circumference of the Cu wiring 5 and a ground film by CVD, and W covering film 6 is formed. W membrane formation conditions at this time make sample temperature 200-400 degrees C, and are WF6. H2 It mixes and a membrane formation room is supplied, and an interface reaction becomes rate-limiting by setting gas ** at this time to 1 or less Torr, and it becomes possible to carry out a selective growth only to Cu and the barrier material alloy film side of a ground. furthermore -- the case where this wiring structure is multilayered -- W covering film 6 top -- SiO2 etc. -- what is necessary is to prepare an insulator layer and just to produce similarly the wiring structure which consists of the Mn film 3, the W film 4, Cu wiring 5, and a W covering film 6 on it

[0011]

[Table 1]

バリア材料	トラップ材料	Cu濃度(相対比)	備考
Ta (900Å)	なし	1	比較例
Zr (900Å)	なし	2	比較例
W (500Å)	Mg (400Å)	0.41	実施例
W (600Å)	Mn (300Å)	0.45	実施例
Ta (600Å)	Mn (300Å)	0.55	実施例

[0012]

[Effect of the Invention] Thus, Cu wiring structure of the semiconductor which can suppress diffusion of Cu was realizable to Cu wiring in the wiring structure of a detailed semiconductor integrated circuit by preparing trap layers, such as barrier layers, such as Ta or W, and Mg, or Mn. Therefore, specific resistance is smaller than aluminum alloy, and a industrial meaning of this Cu wiring excellent in electromigration-proof is very large.

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TECHNICAL FIELD

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TECHNICAL PROBLEM

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MEANS

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OPERATION

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EXAMPLE

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the cross section of Cu wiring structure of this invention.

[Description of Notations]

1 Si Substrate 2 Insulator Layer

3 Mn Film 4 W Film

5 Cu Wiring 6 W Enveloping Layer

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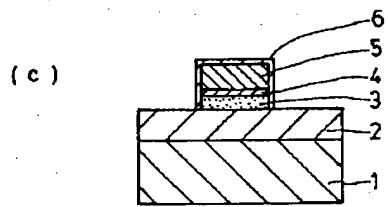
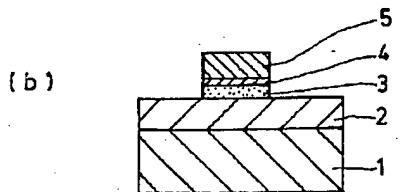
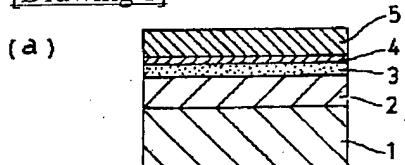
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DRAWINGS

[Drawing 1]



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